1 Proceedings of the 45th annual conference on Design automation

Limor Fix

June 2008 **DAC '08:** Proceedings of the 45th annual conference on Design

Publisher: ACM

Additional Information: full citation, abstract

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citatio

Welcome to the 45th Design Automation Conference and the City of Ana premier event for the electronic design community. It offers the industr prestigious technical conference in combination with the biggest exhibiti

2 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **Transactions on Design Automation of Electronic Syste** Volume 1 Issue 1

Publisher: ACM

Full text available: Pdf (550.02 KB) Additional Information: full citation, abstract, referer terms

Bibliometrics: Downloads (6 Weeks): 53, Downloads (12 Months): 424, Citatio

Low power has emerged as a principal theme in today's electronics indu low power has caused a major paradigm shift in which power dissipatior as performance and area. This article presents an in-depth survey of CA methodologies ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of power dissipation, energy-delay product, gated clocks, layout, low powe power synthesis, lower-power design, power analysis and estimation, p management, power minimization and management, probabilistic analy insulator technology, statistical sampling, switched capacitance, switchi symbolic simulation, synthesis, system design

3 Fast false path identification based on functional unsensitizability usi information

Yuki Yoshikawa, Satoshi Ohtake, Tomoo Inoue, Hideo Fujiwara

January 2009 **ASP-DAC '09:** Proceedings of the 2009 Conference on Asia a Design Automation

Publisher: IEEE Press

Full text available: Pdf (253.93 KB) Additional Information: full citation, abstract, referer

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 2, Citation C

In this paper, we propose a method for identifying false paths based on unsensitizability of path delay faults. By using RTL structural informatio gate level paths are bound into an RTL path and the bundle of them car

4 Towards automated ECOs in FPGAs

Andrew C. Ling, Stephen D. Brown, Jianwen Zhu, Sean Safarpour
February 2009 **FPGA '09:** Proceeding of the ACM/SIGDA international symp programmable gate arrays

Publisher: ACM

Full text available: Pdf (724.09 KB) Additional Information: full citation, abstract, referer

Bibliometrics: Downloads (6 Weeks): 37, Downloads (12 Months): 37, Citation

During the FPGA design flow, engineering change orders (ECOs) have b essential methodology to apply late-stage specification changes and bu beneficial since they are applied directly to a place-and-routed netlist w

Keywords: boolean satisfiability, fpga, optimization, pst, resynthesis

5 Gate-level test generation for sequential circuits

Kwang-Ting Cheng
October 1996 **Transactions on Design Automation of Electronic Syste** Volume 1 Issue 4

Publisher: ACM

Full text available: Pdf (448.19 KB) Additional Information: full citation, abstract, referer terms

Bibliometrics: Downloads (6 Weeks): 13, Downloads (12 Months): 109, Citatio

This paper discusses the gate-level automatic test pattern generation (A and techniques for sequential circuits. The basic concepts, examples, ac limitations of representative methods are reviewed in detail. The relatio

Keywords: IC testing, automatic test generation, sequential circuit tes testing

6 Hardware-accelerated path-delay fault grading of functional test proc processor-based systems

Paolo Bernardi, Michelangelo Grosso, Matteo Sonza Reorda
March 2007 **GLSVLSI '07:** Proceedings of the 17th ACM Great Lakes symp

Publisher: ACM

Full text available: Pdf (369.21 KB) Additional Information: full citation, abstract, referer

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 31, Citation

The path-delay fault simulation of functional tests on complex circuits s processor-based systems is a daunting task. The amount of computing memory needed for verifying or grading functional test programs capab employing ...

Keywords: FPGA, fault-emulation, path-delay, software-based testing

7 Evolution of synthetic RTL benchmark circuits with predefined testab
Tomas Pecenka, Lukas Sekanina, Zdenek Kotasek
July 2008 **Transactions on Design Automation of Electronic Systems** Volume 13 Issue 3
Publisher: ACM
Full text available: Pdf (502.82 KB) Additional Information: full citation, abstract, referer

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 92, Citation

This article presents a new real-world application of evolutionary compu digital-circuits testing. A method is described which enables to evolve la benchmark circuits with a predefined structure and testability. Using ...

Keywords: Benchmark circuit, evolvable hardware, testability analysis

8 Formal verification in hardware design: a survey
Christoph Kern, Mark R. Greenstreet
April 1999 **Transactions on Design Automation of Electronic Systems** Volume 4 Issue 2
Publisher: ACM
Full text available: Pdf (411.53 KB) Additional Information: full citation, abstract, referer terms

Bibliometrics: Downloads (6 Weeks): 41, Downloads (12 Months): 353, Citatio

In recent years, formal methods have emerged as an alternative approa the quality and correctness of hardware designs, overcoming some of th traditional validation techniques such as simulation and testing. There a

Keywords: case studies, formal methods, formal verification, hardware language containment, model checking, survey, theorem proving

9 Large-scale circuit placement
Jason Cong, Joseph R. Shinnerl, Min Xie, Tim Kong, Xin Yuan
April 2005 **Transactions on Design Automation of Electronic Systems** Volume 10 Issue 2
Publisher: ACM
Full text available: Pdf (428.15 KB) Additional Information: full citation, abstract, referer terms

Bibliometrics: Downloads (6 Weeks): 12, Downloads (12 Months): 92, Citation

Placement is one of the most important steps in the RTL-to-GDSII synth directly defines the interconnects, which have become the bottleneck in system performance in deep submicron technologies. The placement pr

Keywords: Placement, large-scale optimization, optimality, scalability

10 Congestion-Aware Logic Synthesis

D. Pandini, L. Pileggi, A. Strojwas
March 2002 **DATE '02:** Proceedings of the conference on Design, automatic Europe
Publisher: IEEE Computer Society
Full text available: Pdf (181.11 KB) Additional Information: full citation, abstract, cited b

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 14, Citation (

In this era of Deep Sub-Micron (DSM) technologies, the impact ofinterc becoming increasingly important as it relates tointegrated circuit (IC) fu performance. In thetraditional top-down IC design flow, interconnect ef

11 RTL Power Optimization with Gate-Level Accuracy
Qi Wang, Sumit Roy
November 2003 **ICCAD '03:** Proceedings of the 2003 IEEE/ACM internation Computer-aided design
Publisher: IEEE Computer Society
Full text available: Pdf (167.94 KB) Additional Information: full citation, abstract, referer

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 30, Citation (

Traditional RTL power optimization techniques committransformations a on the estimation of area, delayand power. However, because of inadeq delayinformation, the power optimization transformations applied atthe

12 A routing approach to reduce glitches in low power FPGAs
Quang Dinh, Deming Chen, Martin D.F. Wong
March 2009 **ISPD '09:** Proceedings of the 2009 international symposium or
Publisher: ACM
Full text available: Pdf (591.14 KB) Additional Information: full citation, abstract, referer

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 2, Citation C

Glitches (spurious transitions) are common in electronic circuits. In this a novel approach to reduce dynamic power in FPGAs by reducing glitche routing step. This approach involves finding alternative routes for early-

Keywords: fpgas, glitch reduction, low power, path balancing, routing

13 Circuit-aware architectural simulation
Seokwoo Lee, Shidhartha Das, Valeria Bertacco, Todd Austin, David Blaauv
June 2004 **DAC '04:** Proceedings of the 41st annual conference on Design a
Publisher: ACM
Full text available: Pdf (291.91 KB) Additional Information: full citation, abstract, referer terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 20, Citation (

Architectural simulation has achieved a prominent role in the system de providing designers the ability to quickly examine a wide variety of desi However, the recent trend in system design toward architectures that re level ...

Keywords: architectural simulation, circuit simulation, computer syster high-performance simulation

14 Layout-driven RTL binding techniques for high-level synthesis using estimators

Min Xu, Fadi J. Kurdahi

October 1997 **Transactions on Design Automation of Electronic Syste** Volume 2 Issue 4

Publisher: ACM

Full text available: Pdf (1.20 MB) Additional Information: full citation, abstract, referer terms

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 60, Citation (

The importance of effective and efficient accounting of layout effects is ' High-Level Synthesis (HLS), since it allows more realistic exploration of and the generation of solutions with predictable metrics. This feature ...

Keywords: FPGAs, binding, floorplan, high-level synthesis

15 IP-block-based design environment for high-throughput VLSI dedicat processing systems

Nacer-Eddine Zergainoh, Katalin Popovici, Ahmed Jerraya, Pascal Urard

January 2005 **ASP-DAC '05:** Proceedings of the 2005 conference on Asia S design automation

Publisher: ACM

Full text available: Pdf (553.38 KB) Additional Information: full citation, abstract, referer

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 26, Citation (

The Growing requirement on the correct design of a high performance D short time force us to use IP's in many design. In this paper, we propos block based design environment for high throughput VLSI Systems. The generates ...

16 A high-level clustering algorithm targeting dual V_{dd} FPGAs

Rajarshi Mukherjee, Song Liu, Seda Ogrenci Memik, Somsubhra Mondal

September 2008 **Transactions on Design Automation of Electronic Sys (TODAES)** , Volume 13 Issue 4

Publisher: ACM

Full text available: Pdf (310.88 KB) Additional Information: full citation, abstract, referer

Bibliometrics: Downloads (6 Weeks): 23, Downloads (12 Months): 110, Citatio

Recent advanced power optimizations deployed in commercial FPGAs, la towards FPGA devices that can be integrated into ultra low power syste we present a high-level design tool to support the process of mapping a

Keywords: Dynamic power, clustering, field programmable gate arrays placement, voltage scaling

17 Register-transfer level functional scan for hierarchical designs

Ho Fai Ko, Qiang Xu, Nicola Nicolici

January 2005 **ASP-DAC '05:** Proceedings of the 2005 conference on Asia S design automation
Publisher: ACM
Full text available: Pdf (410.04 KB) Additional Information: full citation, abstract, referer

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 11, Citation (

This paper discusses the potential benefits of inserting scan chains (SCs designs at the register-transfer level (RTL) of design abstraction. Using for functional scan chain design, it is shown how tight timing constraints

18 Power-aware clock tree planning
Monica Donno, Enrico Macii, Luca Mazzoni
April 2004 **ISPD '04:** Proceedings of the 2004 international symposium on
Publisher: ACM
Full text available: Pdf (299.89 KB) Additional Information: full citation, abstract, referer terms

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 76, Citation (

Modern processors and SoCs require the adoption of power-oriented de the implications that power consumption may have on reliability, cost a manufacturability of integrated circuits featuring nanometric technologie power ...

Keywords: clock tree synthesis and routing, digital design, low-power design and optimization

19 Compatibility path based binding algorithm for interconnect reductior synthesis
Taemin Kim, Xun Liu
November 2007 **ICCAD '07:** Proceedings of the 2007 IEEE/ACM internation Computer-aided design
Publisher: IEEE Press
Full text available: Pdf (551.87 KB) Additional Information: full citation, abstract, referer

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 85, Citation

This paper describes a register and functional unit (FU) binding algorithi synthesis. Our algorithm targets the reduction of multiplexer inputs. Sir connect multiple inputs to FUs or registers, the multiplexer count is a ...

20 Scalable trajectory methods for on-demand analog macromodel extr
Saurabh K. Tiwary, Rob A. Rutenbar
June 2005 **DAC '05:** Proceedings of the 42nd annual conference on Design
Publisher: ACM
Full text available: Pdf (1.10 MB) Additional Information: full citation, abstract, referer terms

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 27, Citation (

Trajectory methods sample the state trajectory of a circuit as it simulat domain, and build macromodels by reducing and interpolating among ...

Keywords: SPICE, analog, circuit, macromodel, trajectory method

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